TRANSLATION FROM JAPANESE

(19) Japanese Patent Office (JP) (12) Unexamined Patent Gazette (A) (11) Unexamined Patent Application (Tokkai Hei) No. **7-218581**
(43) Disclosure Date: August 18, 1995

(51) Int.Cl.[6]	Class. Symbols	Internal Office Registr. Nos.	F I	Technical Display Location
G 01 R 31/26	Z			
	H			
H 01 L 21/02	Z			
21/66	G	7630-4M		
21/68	A			

Request for Examination: Not submitted Number of Claims: 5 OL (Total of 9 pages [in original])

(21) Application No.: Tokugan Hei 6-8377
(22) Filing Date: January 28, 1994

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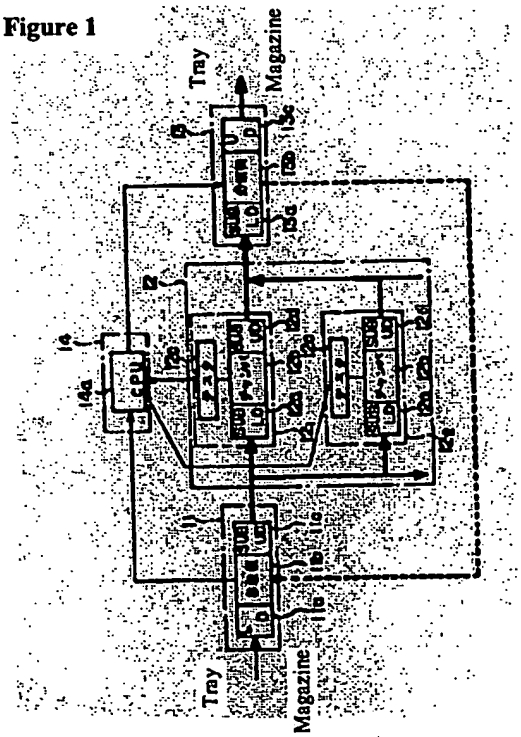
(54) [Title of the Invention] Processing Device for Semiconductor Devices and the Processing Method Thereof

(57) [Summary]

[Object] The most important characteristic of the present invention is to be able to improve cost performance relating to testing for a test handler system that performs product testing of semiconductor component packages using a sub-substrate for which multiple sockets are prepared.

[Structure] For example, sub-loader 12a and sub-unloader 12d that form test unit 12 are prepared for each handler 121, 122, and so on. Then, loader unit 11 that mounts semiconductor component packages into each socket on the sub-substrate and unloader unit 13 that removes the semiconductor component packages from each socket on the sub-substrate and sorts them according to the test results from test unit 12 are separated from this test unit 12. In this way, by treating each unit as an independent device, the structure allows test unit 12 to be changed according to the test time of tester 12c.

Figure 1



[Claims]

[Claim 1] A processing device for semiconductor devices equipped with:

a transfer mechanism composed from a receiving unit that receives semiconductor devices to be processed, a transfer unit that transfers said semiconductor devices received at the receiving unit onto a processing substrate, and a supply unit that supplies said processing substrates onto which said semiconductor devices are transferred by this transfer unit,

a number of processing mechanisms composed from an intake unit that intakes processing substrates in the sequence they were supplied by said supply unit of this transfer mechanism, a processing unit that performs a designated process in sequence on said semiconductor devices that are transferred onto said processing substrates that have been taken in by the intake unit, and an output unit that outputs said processing substrates for which the process on said semiconductor devices by the processing unit has ended,

and a sorting mechanism composed from an acceptance unit that accepts said processing substrates that have been output by said output unit of this processing mechanism, and a sorting unit that sorts said semiconductor devices on said processing substrates accepted at this acceptance unit according to the processing results at said processing unit of said processing mechanism,

and with an independent structure for each of said mechanisms, being able to increase or reduce the number of said processing mechanisms according to the processing capacity of said processing unit.

[Claim 2] The processing device for semiconductor devices of claim 1 wherein specific identification information is attached to said processing substrate, and the device is further equipped with a control means that controls each of said mechanisms based on this identification information.

[Claim 3] The processing device for semiconductor devices of claim 2 wherein said control means has an algorithm for sorting the applicable semiconductor devices by combining processing results from each processing unit f multiple processing mechanisms that perform different processes on semiconductor devices on said processing substrates.

[Claim 4] The processing device for semiconductor devices of claim 1 that is further equipped with a transport means that transports multiple processing substrates in a batch between each of said mechanisms.

[Claim 5] A processing method for semiconductor devices that:

receives semiconductor devices to be processed using the receiving unit of the transfer mechanism, and transfers said semiconductor devices received by this receiving unit onto a processing substrate by the transfer unit of the transfer mechanism, and supplies said processing substrates on which said semiconductor devices are transferred by this transfer unit by the supply unit of the transfer mechanism,

that intakes in sequence processing substrates supplied by said supply unit of this transfer mechanism using the intake unit of any f the processing mechanisms, and performs a designated process by the processing unit of the processing mechanism on said semiconductor devices transferred onto said processing substrates taken in by this intake unit in sequence, and outputs by an output unit of the processing mechanism said processing substrates for which processing by this processing unit on said semiconductor devices has ended,

and that accepts by the acceptance unit of the sorting mechanism said processing substrates output by said output unit of this processing mechanism, and sorts by the sorting unit of the sorting mechanism said semiconductor devices n said processing substrates accepted by this acceptance unit according to the process results at said processing unit of said processing mechanism.

[Detailed Description of the Invention]

[0001]

[Technological Field of the Invention] The present invention relates to a processing device for semiconductor devices and the processing method thereof that performs a designated process on semiconductor devices, for example, and is particularly used for things such as test handler systems that perform characteristics testing on semiconductor devices.

[0002]

[Prior Art] In recent years, as items that perform characteristics testing of semiconductor devices, test handler systems that perform product tests such as temperature tests on semiconductor

component packages (product to be tested) that are assembled in package form, for example, have been put to practical use.

[0003] Figure 8 shows the schematic structure of a test handler system for performing product testing. This test handler system is constructed as a single unit from a loader unit 1, a test unit 2, and an unloader unit 3, for example, and the semiconductor component packages are taken from tray 4 by robot 1a of the aforementioned loader unit 1 and transferred onto sub-substrate 5, the sub-substrate 5 is transported in the arrow direction in the figure by a conveyor and sent to one of the chambers (constant temperature bath) 2a or 2b of test unit 2, and after temperature testing is done by a tester that is not illustrated, this is further transported in the arrow direction shown in the figure.

[0004] Then, semiconductor component packages are taken from sub-substrate 5 by robot 3a of the aforementioned unloader unit 3, and these are sorted according to the aforementioned test results and housed in multiple different trays 6.

[0005] The empty sub-substrates 5 for which removal of semiconductor component packages has ended is further transported in the arrow direction in the figure, and are retrieved at the aforementioned loader unit 1 to be used repeatedly for product testing thereafter.

[0006] In this case, test unit 2 has two chambers 2a and 2b, and by transporting in parallel sub-substrates 5 to the two chambers 2a and 2b which are controlled at the same temperature, the processing capacity of test unit 2 is increased, making it possible to perform processing efficiently (simultaneous parallel processing).

[0007] For example, a maximum of 16 semiconductor component packages can be mounted on one sub-substrate 5, making it possible to supply 64 semiconductor component packages at once for product testing.

[0008] Also, as with this system, in a case of a single unit structure test handler system (single unit handler) made by placing a loader unit 1 or unloader unit 3 on both sides of test unit 2, as shown in figure 9, for example, with one chamber 2a of test unit 2 at a low temperature (LT chamber) and the other chamber 2b at a high temperature (HT chamber), by transporting sub-substrates 5 serially between these two chambers 2a and 2b, it is possible to c ntinuously

perform a low temperature test and high temperature test on semiconductor component packages on sub-substrate 5.

[0009] The test handler system described above had problems such as those noted below, however. Specifically, prior art test handler systems had a single unit structure made from a loader unit 1, a test unit 2 that has two chambers 2a and 2b, and an unloader unit 3, so there was the disadvantage of having poor operating efficiency as a system.

[0010] For example, because it is not possible to change the structure of test unit 2, in other words because it is not possible to increase the number f testers, as the time required for product testing (test time) lengthens, the operating efficiency of loader unit 1 and unloader unit 3 is reduced.

[0011] Also, as test time shortens, the overall processing capacity of the system is limited by the processing capacity of loader unit 1 and unloader unit 3, there are limits to the capacity to sort the semiconductor component packages transferred onto sub-substrate 5 by loader unit 1 and to the capacity to sort semiconductor component packages removed from sub-substrate 5 by unloader unit 3, and it is not possible to exceed these limits and operate the tester.

[0012] Because of this, even if the test time shortens, it is not possible to improve the operating efficiency of test unit 2 (tester) (see figure 7). Also, when loader unit 1 or unloader unit 3 breaks down, the operation of test unit 2 stops, in ther words, the operating efficiency of the tester drips when either loader unit 1 or unloader unit 3 breaks down. This kind of surplus capacity (drop in operating efficiency) of test unit 2 or loader unit 1 or unloader unit 3 becomes an excessive facility investment, resulting in increased testing costs.

[0013]

[Problems the Invention Attempts to Solve] As described above, in the past, drops in operating efficiency occurred easily, leading to the problem of increased test costs such as in the form f excessive facility investment. In light of this, the goal of the present invention is to provide a processing device for semiconductor devices and the processing method thereof for which it is possible to make facilities investment according to the processing capacity, to reduce facilities expenses, and reduce processing c sts.

[0014]

[Means t S lve the Problems] To achieve the

goal noted above, the processing device for semiconductor devices of the present invention has a structure equipped with a transfer mechanism composed from a receiving unit that receives semiconductor devices to be processed, a transfer unit that transfers said semiconductor devices received at the receiving unit onto a processing substrate, and a supply unit that supplies said processing substrates onto which said semiconductor devices are transferred by this transfer unit, a number of processing mechanisms composed from an intake unit that intakes processing substrates in the sequence they were supplied by said supply unit of this transfer mechanism, a processing unit that performs a designated process in sequence on said semiconductor devices that are transferred onto said processing substrates that have been taken in by the intake unit, and an output unit that outputs said processing substrates for which the process on said semiconductor devices by the processing unit has ended, and a sorting mechanism composed from an acceptance unit that accepts said processing substrates that have been output by said output unit of this processing mechanism, and a sorting unit that sorts said semiconductor devices n said processing substrates accepted at this acceptance unit according to the processing results at said processing unit of said processing mechanism, and with an independent structure for each of said mechanisms, being able to increase or reduce the number of said processing mechanisms according to the processing capacity of said processing unit.

[0015] Also, the processing method of semiconductor devices of the present invention is a method that receives semiconductor devices to be processed using the receiving unit of the transfer mechanism, and transfers said semiconductor devices received by this receiving unit onto a processing substrate by the transfer unit of the transfer mechanism, and supplies said processing substrates on which said semiconductor devices are transferred by this transfer unit by the supply unit of the transfer mechanism, that intakes in sequence processing substrates supplied by said supply unit of this transfer mechanism using the intake unit of any of the processing mechanisms, and performs a designated process by the processing unit of the processing mechanism on said semic nductor devices transferred ont said processing substrates taken in by this intake unit in sequence, and outputs by an utput unit of the processing mechanism said processing substrates for which processing by this processing unit on said semiconductor devices has ended, and that accepts by the acceptance unit of the sorting mechanism said processing substrates output by said output unit of this processing mechanism, and sorts by the sorting unit of the sorting mechanism said semiconductor devices n said processing substrates accepted by this acceptance unit according to the process results at said processing unit of said processing mechanism.

[0016]

[Effect] The present invention has a structure whereby each mechanism is independent by using the means noted above, and it is possible to increase or decrease the number of processing mechanisms according to processing capabilities, so it is possible to improve cost performance relating to processing.

[0017]

[Working Examples] In the following, we will explain a working example of the present invention while referring to the figures. Figure 1 gives a conceptual view of the schematic structure of the test handler system of the present invention.

[0018] Specifically, this test handler system is formed, from four independent devices, including loader unit (transfer mechanism) 11 that transfers semiconductor component packages (semiconductor devices) as the products to be tested onto a sub-substrate (SUB substrate) as the processing substrate to be described later, a test unit 12 that executes a designated product test on semiconductor component packages transferred onto the aforementioned sub-substrate, an unloader unit (sorting mechanism) 13 that removes semiconductor component packages from the aforementioned sub-substrates and sorts them according to the test results, and a block computer (B/C) 14 as a control means that controls each unit.

[0019] Loader unit 11 is composed from loader (LD) 11a as a receiving unit that receives semiconductor component packages from trays or magazines (not illustrated), transfer apparatus 11b as a transfer unit that transfers semiconductor component packages received by this loader 11a onto sub-substrates, and sub-unloader (SUB UD) 11c as a supply unit that supplies sub-substrates to which semiconductor component packages were

transferred by transfer apparatus 11b to the aforementioned test unit 12.

[0020] Test unit 12 is composed from multiple handlers (processing mechanisms) 121, 122, and so on that perform designated product testing including characteristics tests such as low temperature tests or high temperature tests on semiconductor component packages on sub-substrates supplied from the aforementioned loader unit 11.

[0021] Each of the aforementioned handlers 121, 122, and so on is composed from items such as sub loader (SUB LD) 12a as an intake unit that intakes in sequence sub-substrates supplied by the aforementioned sub-unloader 11c of the aforementioned loader unit 11, tester 12c as a processing unit that sends sub-substrates taken in by sub-loader 12a in sequence into chamber (constant temperature bath) 12b and tests semiconductor component packages in that temperature atmosphere, and sub-unloader 12d as an output unit that outputs the aforementioned sub-substrates for which testing by tester 12c has ended toward unloader unit 13 at a latter step.

[0022] These handlers 21, 122, and so on can be suitably increased or decreased according to the processing capacity (test time of tester 12c) of the concerned test unit 12.

[0023] Unloader unit 13 is composed from a sub-loader 13a as an acceptance unit that accepts sub-substrates output by the sub-unloader 12d of each handler 121, 122, and so on of the aforementioned test unit 12, sorter 13b as a sorting unit that removes semiconductor component packages on sub-substrates accepted by this sub-loader 13a and sorts these according to the test results of tester 12c of each handler 121, 122, and so on of the aforementioned test unit 12, and unloader (UD) 13c that houses semiconductor component packages sorted by this sorter 13b in trays or magazines (not illustrated).

[0024] Block computer 14 is made to control the product name, lot number, test results by tester 12c, and sorting instructions to sorter 13b of the aforementioned unloader unit 13 in correspondence to these test results for semiconductor component packages for which product testing is done based on the control of CPU 14a, for example, based on things such as specific identification information (described later) given to each sub-substrate.

[0025] Here, we will explain a sub-substrate used for product tests by the test handler system described above. Figure 2 shows the schematic structure of a sub-substrate. Figure 2 (a) is a planar view of a sub-substrate, and figure 2 (b) is a side view of this.

[0026] The sub-substrate 21 with which handling of semiconductor component packages is performed has a structure whereby multiple (in this case 16) sockets 22 are provided for mounting semiconductor component packages such as SOJ (Small Outline J-leaded Package) or TSOP (Thin Small Outline Package) supplied for product tests on printed substrate 21a on which a circuit pattern (not illustrated) is routed, for example.

[0027] At one end of the aforementioned sub-substrate 21 is attached, for example, bar code information 23 that records the aforementioned specific identification information for each sub-substrate 21. Specifically, by supplying this kind of sub-substrate 21 to each handler 121, 122, and so on of test unit 12, testing can be done on 16 semiconductor component packages at once by each tester 12c.

[0028] Figure 3 shows the schematic structure of socket 22. Figure 3 (a) is a top surface view of socket 22, and figure 3 (b) is a side view of this with a partial cut out.

[0029] Socket 22 has a structure such that when cap 22a is pressed down, the contact terminal 22c of contactor 22b that is contacted with each electrode lead of the semiconductor component package mounted within socket 22 expands outward. In this state, after the semiconductor component package is mounted within socket 22, by returning cap 22a to its original position, each electrode lead of the semiconductor component package and each contact terminal 22c of contactor 22b contact each other.

[0030] Then, the reverse contact terminal 22c side of the aforementioned contactor 22b projects fr m the bottom surface of socket 22 outward (sub-substrate 21 side), becoming external terminal 22d contacted by the test head (not illustrated) of the aforementioned tester 12c.

[0031] Socket 22 is attached and fixed onto the aforementioned sub-substrate 21 by screw 24. The trays used in this working example arrange in a flat manner and house multiple semic nductor component packages for product testing and multiple semiconductor component packages for which product testing has ended, and the

magazines house multiple, stacked semiconductor component packages.

[0032] For a test handler system with the structure described above, first, the semiconductor component packages housed in trays or magazines are received by loader 11a of the aforementioned loader unit 11, and these semiconductor component packages are mounted in sockets 22 on the sub-substrate 21 by transfer apparatus 11b.

[0033] In this way, sub-substrate 21 onto which are transferred multiple semiconductor component packages are supplied in sequence by sub-unloader 11c to each handler 121, 122, and so on of the aforementioned test unit 12.

[0034] The sub-substrates 21 from loader unit 11 are sent in sequence into each chamber 12b by sub-loader 12a after being accepted by sub-loader 12a of each handler 121, 122, and so on.

[0035] Then, in that designated temperature atmosphere, product tests are performed on each semiconductor component package by each tester 12c. After that, the sub-substrates 21 for which product testing on semiconductor component packages by tester 12c is completed are output toward the aforementioned unloader unit 13 by each sub-unloader 12d.

[0036] For the sub-substrates 21 from each handler 121, 122, and so on, by being accepted by sub-loader 13a, the semiconductor component packages mounted in each socket 22 on each sub-substrate 21 are removed by sorter 13b.

[0037] In this case, each semiconductor component package is removed according to the product name, lot number, and test results, etc. based on the sorting instructions from block computer 14 such as bar code information 23.

[0038] Then, each semiconductor component package removed by sorter 13b is sorted and housed in multiple different trays or magazines by unloader 13c.

[0039] The empty sub-substrates 21 for which removal of semiconductor component packages has ended are returned to the aforementioned loader unit 11 and used repeatedly for product tests thereafter. In this way, it becomes easy to build a system for which multiple handlers 121, 122, and so on are placed according to the processing capacity of test unit 12 between loader unit 11 and unl ader unit 13.

[0040] Specifically, considering the test time of tester 12c, test unit 12 is constructed to match the processing capacity of loader unit 11 and unloader unit 13. For example, with a processing capacity of "1" for loader unit 11 and unloader unit 13, when tester 12c of each handler 121, 122, and so on requires 4 times the test time, by constructing test unit 12 from four handlers 121 through 124, even when the test time is long, there is no waiting time, making it possible to operate each unit, and thus improving the operating efficiency of each unit.

[0041] Meanwhile, with a processing capacity f "1" for loader unit 11 and unloader unit 13, for example, when the testers 12c of each handler 121, 122, and so on requires twice the test time, by constructing test unit 12 from two handlers 121 and 122, there is no waiting time even when the test time is shorter, making it possible to operate each unit and to improve the operating efficiency of each unit.

[0042] In fact, by eliminating the waiting time for each unit and being able to efficiently operate each unit, it is possible to eliminate surplus capacity. Because of this, a slight increase in expenses that accompanies structural changes to each unit is unavoidable, but even so, it is ultimately possible to prevent excessive facilities investment.

[0043] For the test handler system of the present invention, intake and output of sub-substrates 21 is possible for each handler 121, 122, and so on, so for example as shown in figure 4, it is possible to construct a system so that multiple sub-substrates 21 can be supplied in a batch to each handler 121, 122, and so on.

[0044] Figure 4 shows an example of a test handler system structure with low temperature and high temperature tests performed in succession on semiconductor component packages. This test handler system is constructed with four independent devices including each of the aforementioned units, specifically a loader unit 11, test unit 12, unloader unit 13, and block computer 14 placed around automatic cassette conveyor path 31.

[0045] In this case, the aforementioned automatic cassette conveyor path 31 conveys multiple units of sub-substrate 21 on which are transferred semiconductor component packages, and conveys sub-substrate cassettes 32 in which are housed multiple sub-substrates 21 as shown in figure 5, for example. The main structural component is a conveyor belt, etc.

[0046] The aforementioned loader unit 11 is composed from elements such as loader 11a that

receives semiconductor component packages housed in trays or magazines (not illustrated), transfer apparatus 11b that transfers semiconductor component packages received by this loader 11a onto sub-substrates 21 taken out from the aforementioned sub-substrate cassette 32, sub-unloader 11c for which sub-substrates 21 onto which semiconductor component packages are transferred by this transfer apparatus 11b are housed within the aforementioned sub-substrate cassette 32, and a cassette handler 11d that conveys sub-substrate cassette 32 on the aforementioned automatic cassette conveyor path 31.

[0047] The aforementioned test unit 12 is formed from multiple handlers 121, 122, 123, 124, and so on that perform tests such as low temperature tests and high temperature tests on semiconductor component packages on sub-substrates 21 housed in the aforementioned sub-substrate cassettes 32 that are conveyed via the aforementioned automatic cassette conveyor path 31.

[0048] Normally, high temperature tests are performed after low temperature tests, but because high temperature tests take a longer time than low temperature tests, here, for one handler 121 for low temperature tests, several times as many, in other words multiple high temperature test handlers 122, 123, 124, and so on are prepared.

[0049] For example, 10 to 20 handlers are prepared when there are semiconductor component packages with a long test time such as a 16 M DRAM. In cases of semiconductor component packages with very short test times such as a high temperature test time that is about two times the low temperature test time, only three handlers are needed (one for low temperature testing, and two for high temperature testing).

[0050] The aforementioned handlers 121, 122, 123, 124, and so on are composed from sub-loader 12a that intakes in sequence multiple sub-substrates 21 housed in the aforementioned sub-substrate cassette 32, chamber 12b in which are placed sub-substrates 21 taken in by this sub-loader 12a, tester 12c that tests semiconductor component packages taken into 12b within that temperature atmosphere, sub-unloader 12d for which the aforementioned sub-substrates 21 for which tests by this tester 12c are finished are housed within the aforementioned sub-substrate cassette 32, and cassette handler 12e that conveys sub-substrate cassette 32 on the aforementioned automatic cassette conveyor path 31.

[0051] Each handler 121, 122, 123, 124, and so on has tw chambers 12b and 12b. For example, of the aforementioned handlers 121, 122, 123, 124, and so on, handler 121 for low temperature testing has two LT chambers (constant temperature bath controlled to a low temperature) 12b and 12b, and handlers 122, 123, 124, and so on for high temperature testing each have two HT chambers (constant temperature bath controlled to a high temperature) 12b and 12b.

[0052] By doing this, by supplying sub-substrates 21 on which are transferred 16 semiconductor component packages each, for example to handlers 121, 122, 123, 124, and so on, it becomes possible to test 32 semiconductor component packages at a time.

[0053] The aforementioned unloader unit 13 is composed from items such as sub-loader 13a that accepts multiple sub-substrates 21 housed in the aforementioned sub-substrate cassette 32, sorter 13b that removes semiconductor component packages on sub-substrates 21 accepted by this sub-loader 13a and sorts them according to the sorting instructions (test results, etc.) from the aforementioned block computer 14, unloader 13c for which semiconductor component packages sorted by sorter 13b are housed in trays r magazines (not illustrated), and a cassette handler 13d that conveys sub-substrate cassettes 32 on the aforementioned automatic cassette conveyor path 31.

[0054] In addition, the aforementioned block computer 14 performs conveyance control of the aforementioned sub-substrate cassettes 32 conveyed on the aforementioned automatic cassette conveyor path 31 and also is constructed to have an algorithm for sorting the concerned semiconductor packages by combining test results from handler 121 for low temperature testing and test results from any of handers 122, 123, 124, and so on for high temperature testing.

[0055] Here, we will give a summary explanation of the cassette handler that conveys sub-substrat cassettes 32 on the aforementioned automatic cassette conveyor path 31. Figure 6 schematically illustrates the structure of cassette handler 11d. Figure 6 (a) is a top view showing the movement of sub-substrate cassette 32 within cassette handler 11d, and figure 6 (b) is a side view f this.

[0056] This cassette handler 11d is formed as a single unit from, for example, sub-substrate loader 41 that takes in sub-substrate cassettes 32

conveyed on automatic cassette convey r path 31 and clears out multiple sub-substrates 21 housed within this cassette 32 in sequence to the aforementioned transfer apparatus 11b, and sub-substrate unloader 42 that returns in sequence into cassette 32 the sub-substrates 21 on which semiconductor component packages have been transferred by the aforementioned transfer apparatus 11b, and sends sub-substrate cassettes 32 which house all sub-substrates 21 onto the aforementioned automatic cassette conveyor path 31.

[0057] Specifically, sub-substrate cassettes 32 are taken into (machine on) cassette handler 11d from position A in the figure and the interiors are moved in sequence. Then, while the up-down position is controlled by elevator 43, one sub-substrate 21 at a time is cleared out in direction B in the figure.

[0058] Sub-substrate cassettes 32 from which all sub-substrates 21 are cleared out are sent to elevator 44. Then, while the up-down position is controlled, sub-substrates 21 onto which semiconductor component packages have been transferred from direction C in the figure are returned one at a time and stored in sequence.

[0059] Sub-substrate cassettes 32 on which all sub-substrates 21 are stored, after being sent to elevator 45, have their interiors moved in sequence and are sent onto automatic cassette conveyor path 31 from position D in the figure (machine off).

[0060] With this working example, cassette handler 11d has sub-substrate loader 41 and sub-substrate unloader 42, both of which can hold 10 sub-substrate cassettes 32 at a time.

[0061] Because of this, by using cassette handler 11d as a buffer, even in a case when trouble occurs with loader unit 11 or unloader unit 13 midway in the operation, for example, it is possible to operate test unit 12 even while that trouble is being solved, improving the operating efficiency of each tester 12c for test unit 12.

[0062] Here, we explained the structure of an example of cassette handler 11d, but cassette handler 12e and 13d have the same structure. In this way, when constructing a test handler system that can supply multiple sub-substrates 21 in a batch, for example as shown in figure 7, when a short test time is possible, a significant improvement in throughput is possible.

[0063] Specifically, with this system, compared with the prior art system, when the test time is shorter than 56 seconds f r example, throughput can be improved, and an approximately 1.60 x increase in efficiency can be attempted when the test time is 30 seconds.

[0064] In fact, with this system, by using automatic conveying, there is an attempt to save labor, and by distributing tests on the same lot over multiple handlers, simultaneous parallel processing is possible, so work time can be shortened.

[0065] As described above, with a structure where the loader unit, test unit, and unloader unit are independent, it is possible to increase and decrease the number of test unit handlers according to the test time of the tester.

[0066] Specifically, for a test handler system that performs product tests on semiconductor component packages using a sub-substrate that has multiple sockets, each handler that makes up the test unit is equipped with a loader and unloader, and the loader unit that mounts semiconductor component packages into each socket on the sub-substrate and the unloader unit that removes semiconductor component packages from each socket on the sub-substrates and sorts them according to test results are constructed to be separate from this test unit.

[0067] By doing this, it is possible to construct the optimal test unit according to the test time of the tester, so it is possible to improve the cost performance relating to testing.

[0068] Therefore, it is possible to prevent an increase in wasteful facilities expenses and to improve the operating efficiency of each unit, making it possible to significantly decrease testing costs.

[0069] For the aforementioned working example, we explained an example of doing a product test using high and low temperature testing, but the present invention is not limited to this, and can easily be applied to items that perform other characteristics tests as well. In addition, it goes without saying that a variety of variation embodiments are possible without straying from the key points of the present invention.

[0070]

[Merits of the Invention] With the present invention described in detail above, it is possible to provide a processing device for semiconductor devices and the processing method thereof for which facilities investment can be made according t processing capacity, and for which facilities expenses can be reduced, while at the same time perating efficiency is improved, and processing

costs are reduced.

[Brief Description of the Figures]

[Figure 1] This is a conceptual diagram that shows the schematic structure of the test handler system of a working example of the present invention.

[Figure 2] This is a diagram that shows a structural example of the sub-substrate used with a test handler system of a working example of the present invention.

[Figure 3] This is a schematic structural diagram showing sockets placed on a sub-substrate.

[Figure 4] This is a block diagram of an example of building a test handler system of a working example of the present invention.

[Figure 5] This is an oblique diagram that schematically shows a sub-substrate cassette used with a test handler system of a working example of the present invention.

[Figure 6] This is a structural diagram that schematically shows a cassette handler used for conveying sub-substrate cassettes of a working example of the present invention.

[Figure 7] This is a diagram that shows the processing capacity of this system of a working example of the present invention compared to a prior art system.

[Figure 8] This is an oblique structural diagram of a test handler system shown to explain the prior art and its problems.

[Figure 9] This is a block diagram that schematically shows an example of building another prior art system shown to explain the prior art and its problems.

[Key]

11 Loader unit
11a Loader
11b Transfer apparatus
11c Sub-unloader
11d Cassette handler
12 Test unit
121, 122Handler
12a Sub-loader
12b Chamber
12c Tester
12d Sub-unloader
12e Cassette handler
13 Unloader unit
13a Sub-loader
13b Sorter
13c Unloader
13d Cassette handler
14 Block computer
21 Sub-substrate
22 Socket
23 Bar code information
31 Automatic cassette conveyor path
32 Sub-substrate cassette

Figure 1

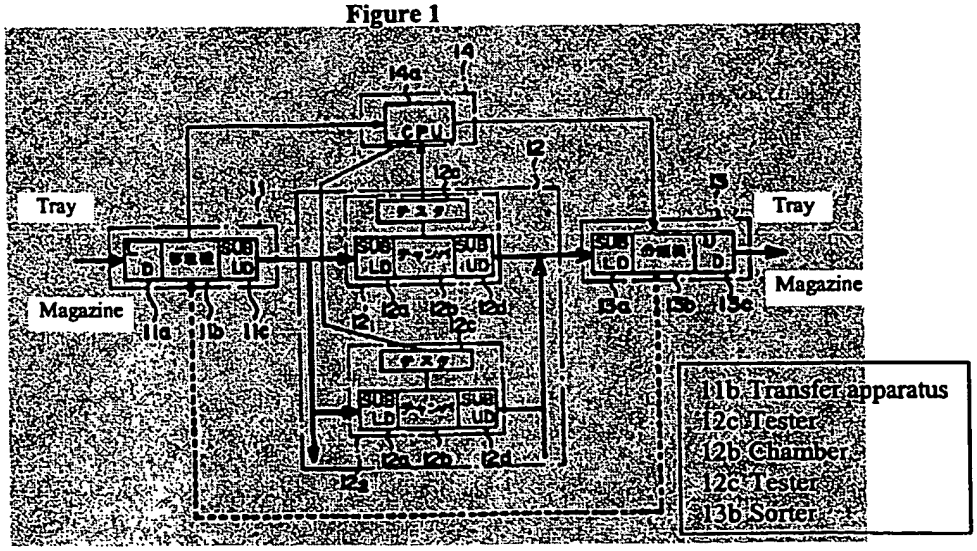


Figure 5

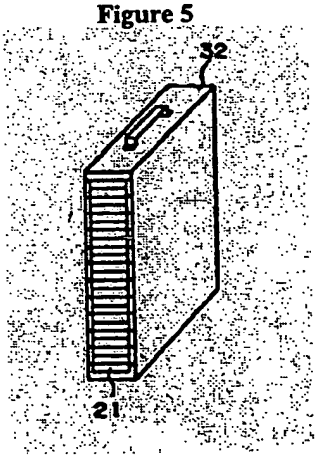


Figure 2

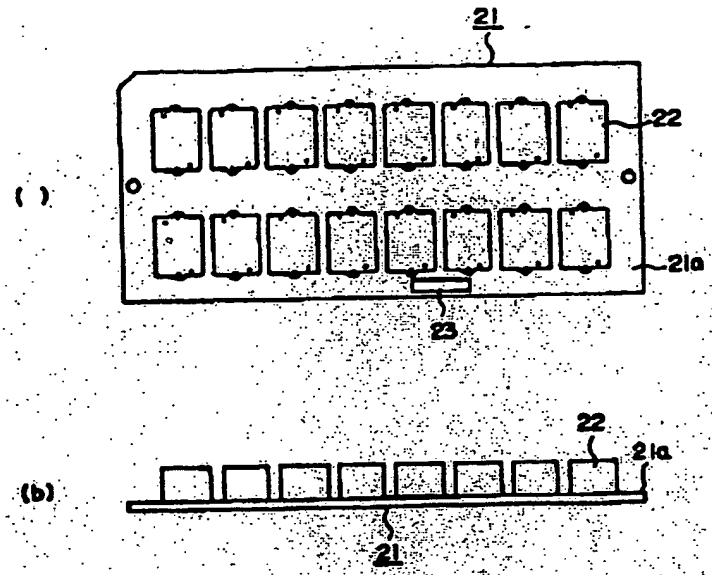
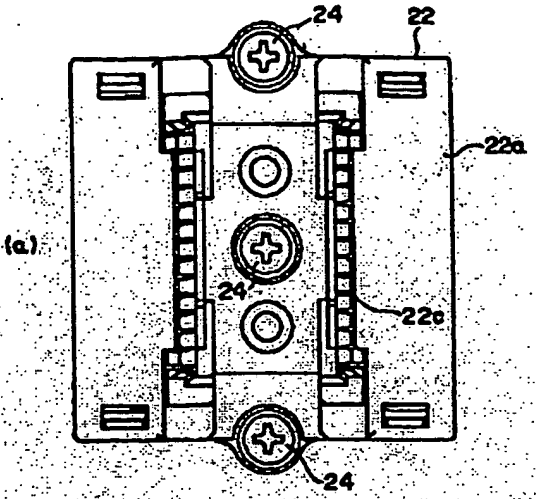


Figure 3



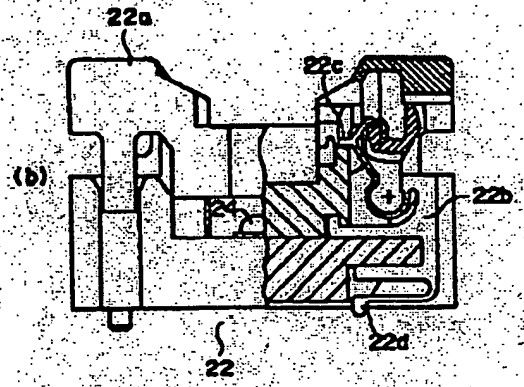
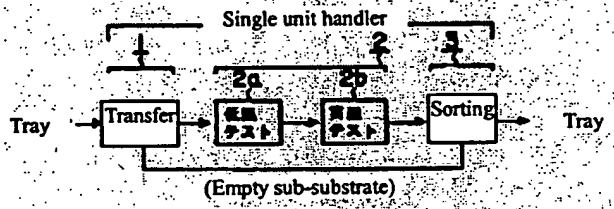
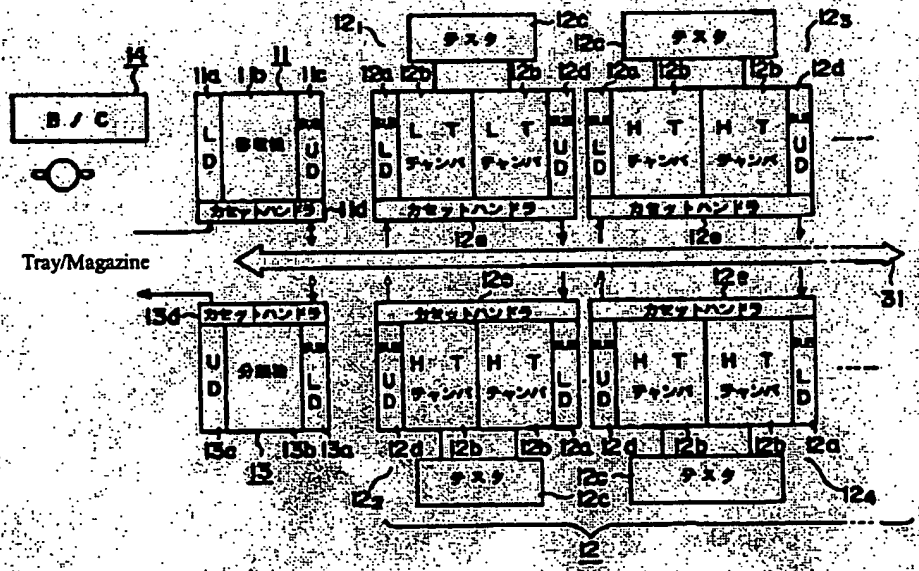


Figure 9



2a Low temperature test
2b High temperature test

Figure 4



12c Tester
11b Transfer apparatus
12b LT chamber
12b HT chamber
11d Cassette handler
12e Cassette handler
13d Cassette handler
13 Sorter

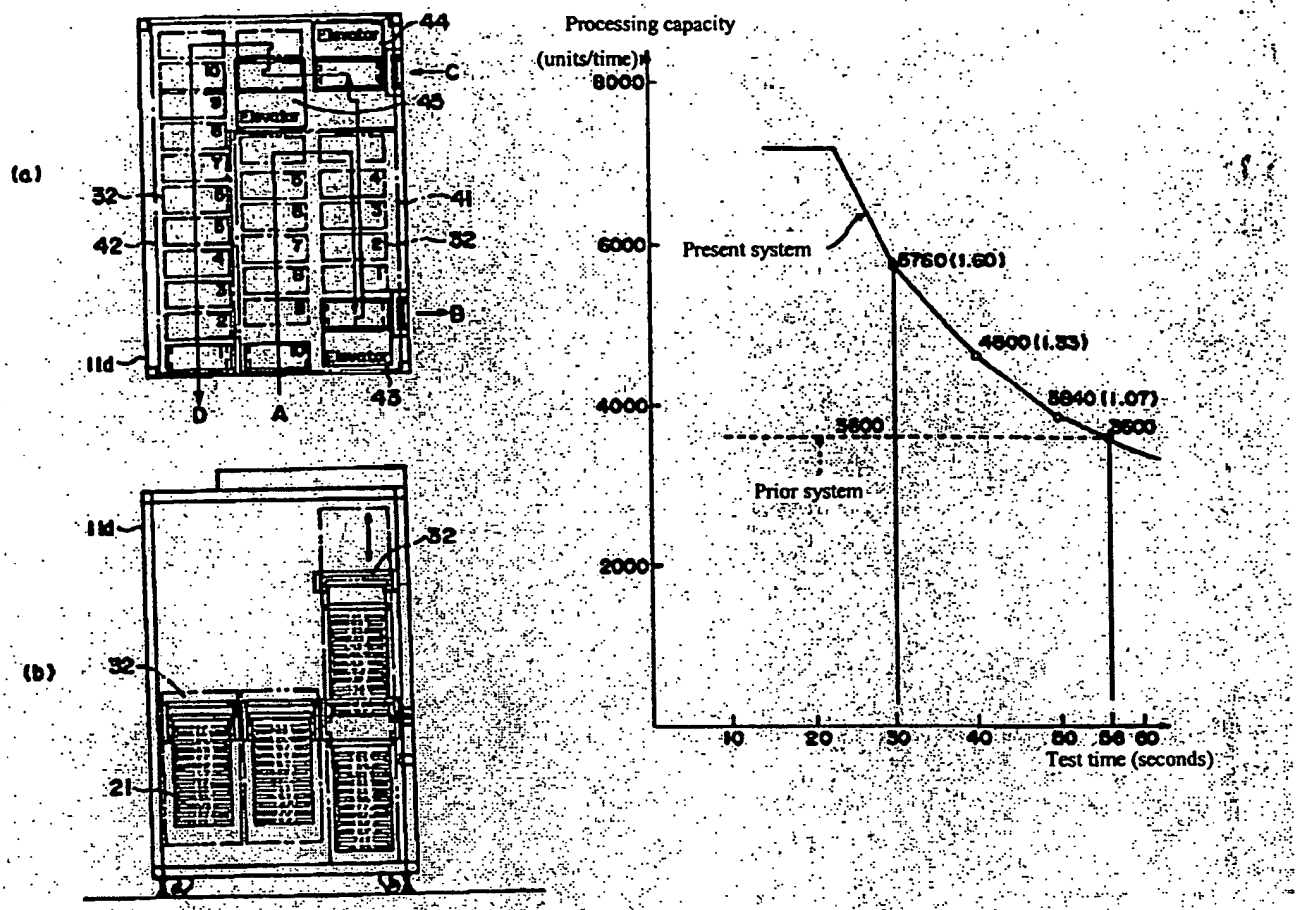
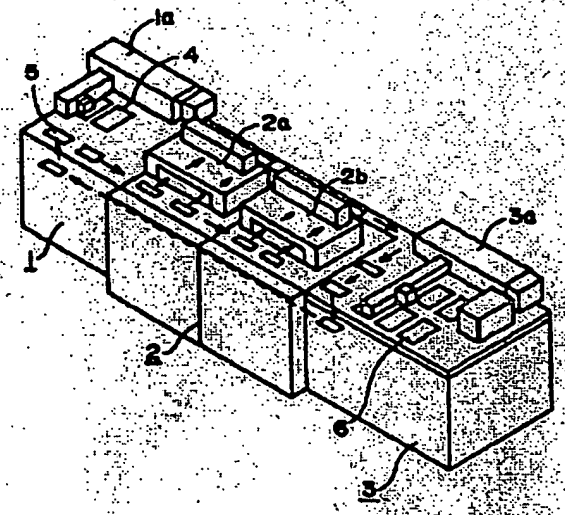

(a)
(b)
44
C
45
41
32
42
52
8
11d
D
A
45
11d
52
32
21
Processing capacity
(units/time)
8000
6000
4000
2000
Present system
5760(1.60)
4800(1.33)
3840(1.07)
3600
3600
Prior system
10
20
30
40
50
60
Test time (seconds)

Figure 8


1a
4
5
2a
2b
3a
1
2
6
3